

Fig. 2

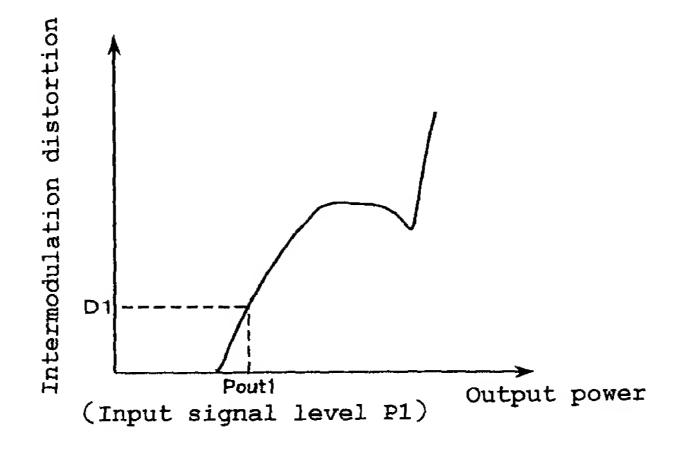
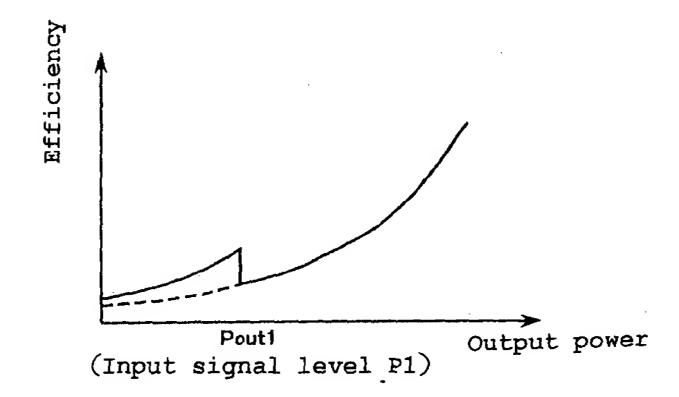


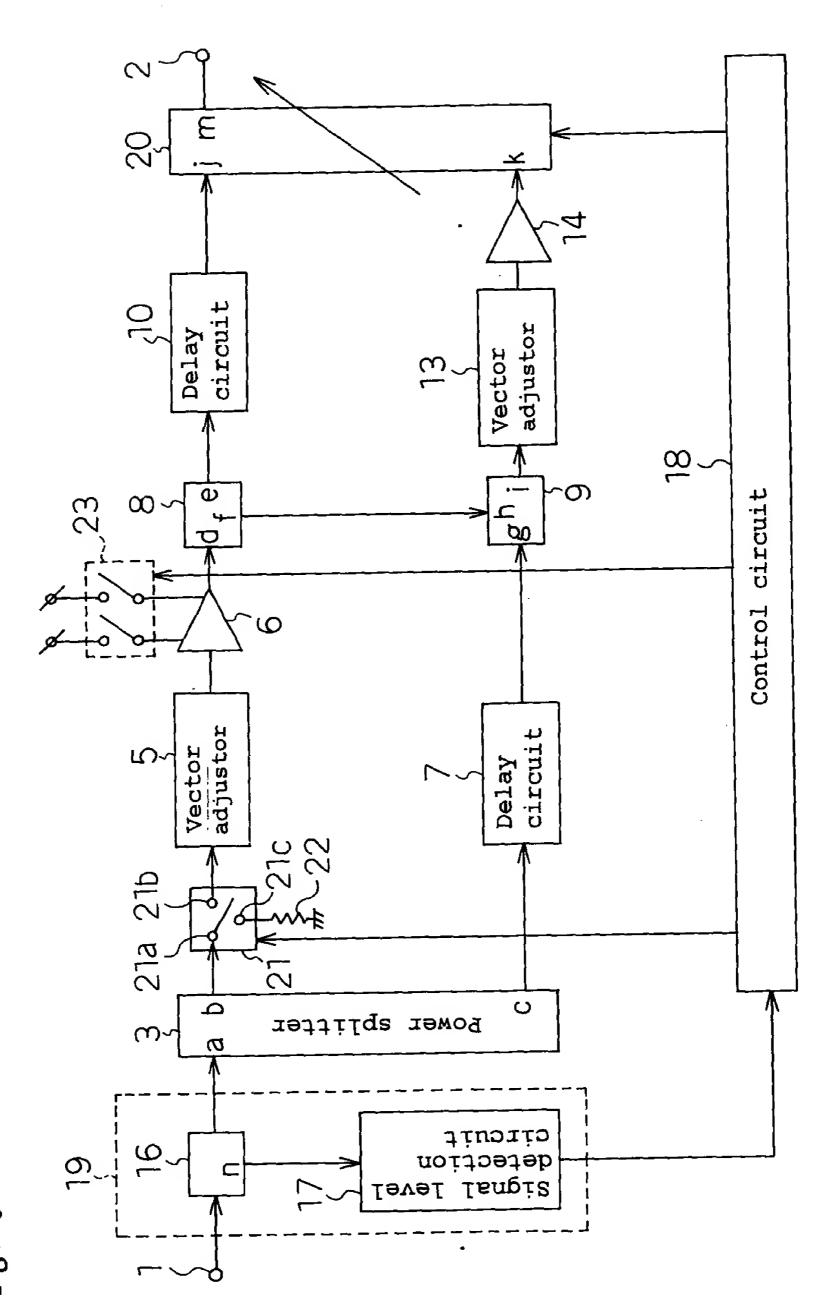
Fig. 3



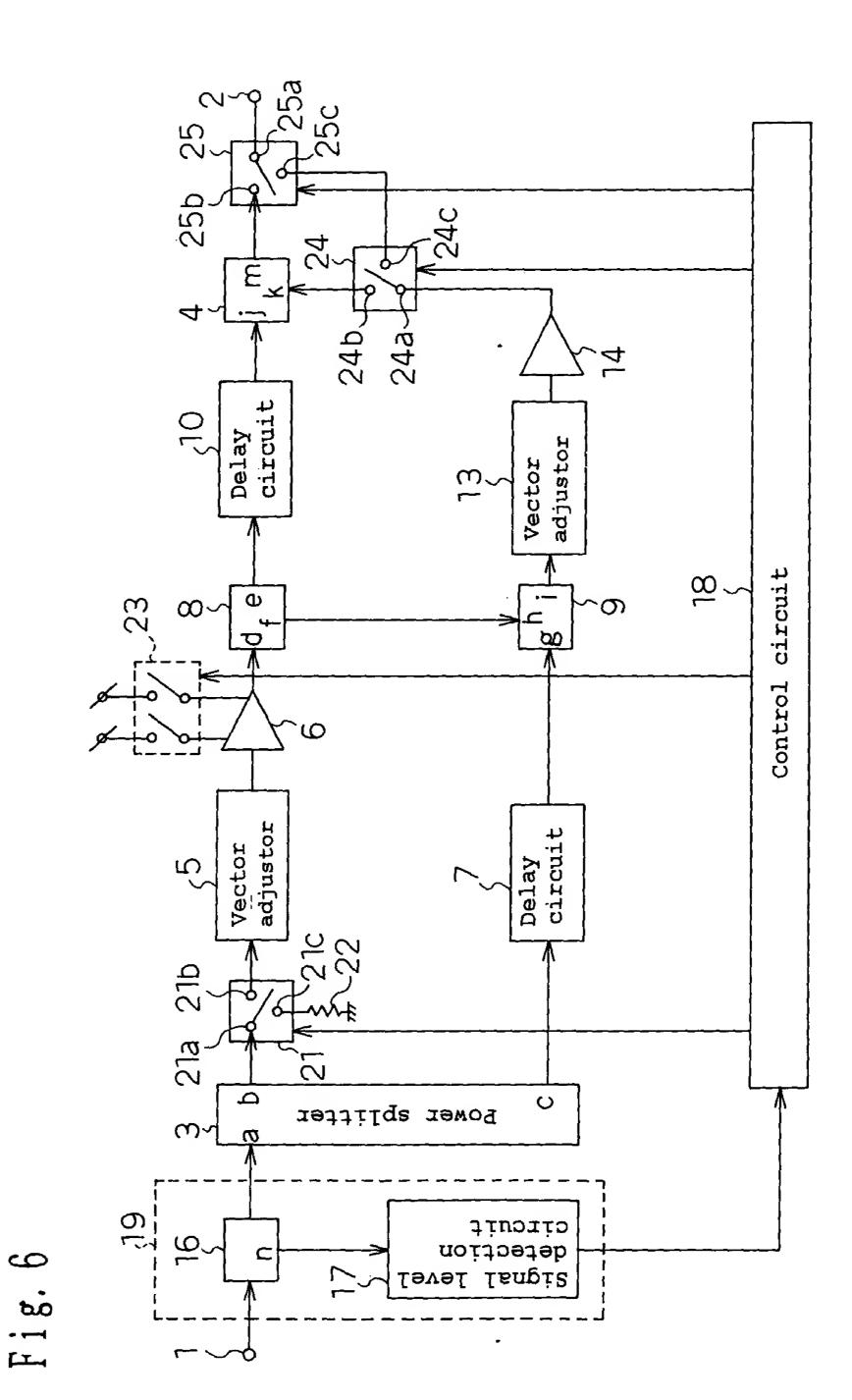
2 Signal level detection circuit 29 26 Power-combiner 4 14 circuit Delay adjustor Vector $\frac{1}{3}$ circuit 9 Φ $\infty \sim$ n g 23 Control 9 Delay circuit adjustor Vector 5 21a \circ Power splitter circuit detection Signal Level

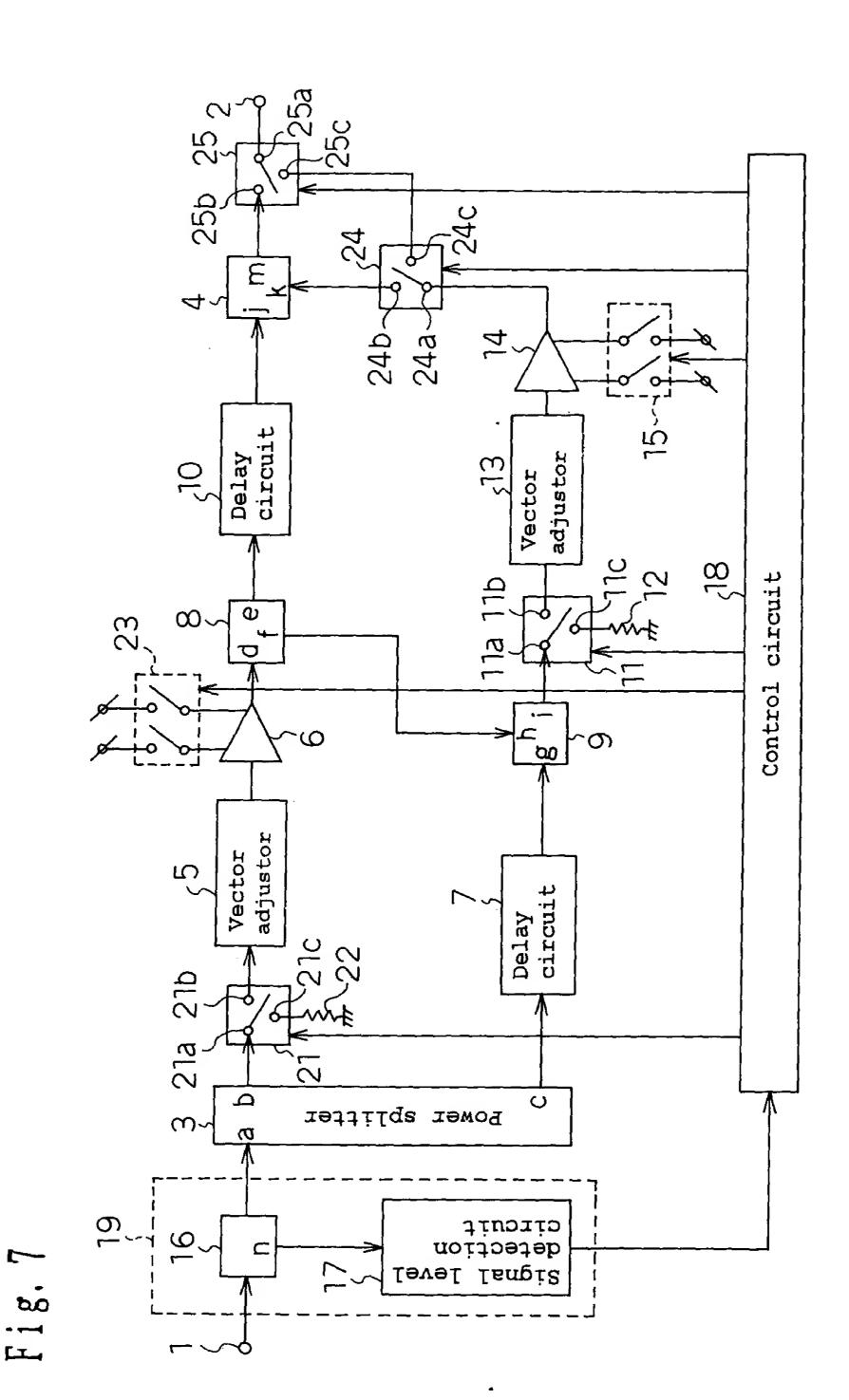
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Fig. 11

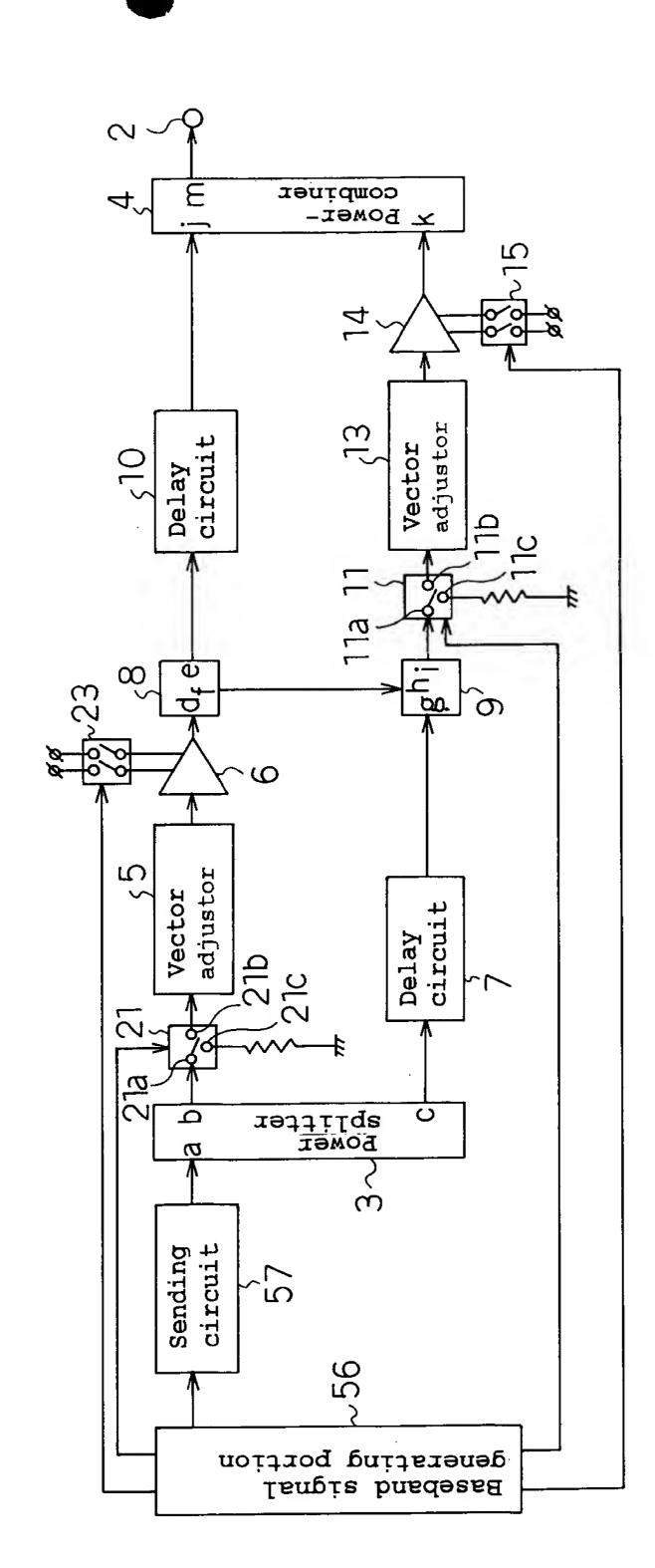


Fig. 12

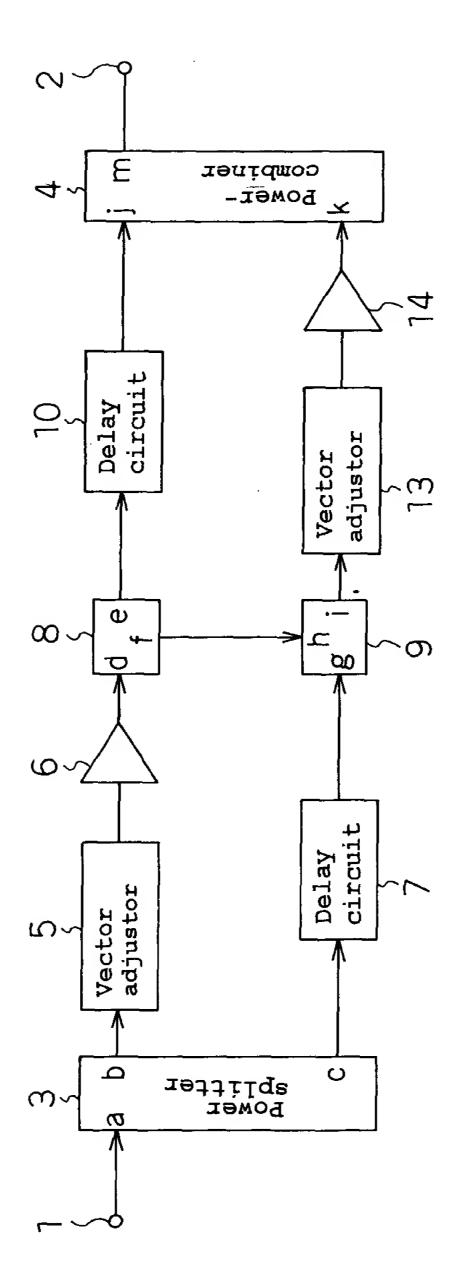


Fig. 13 (a)

Fig. 13 (b)

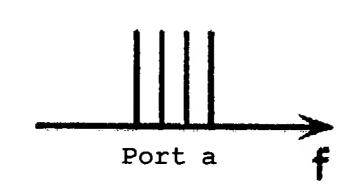
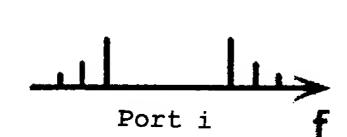


Fig. 13 (c)



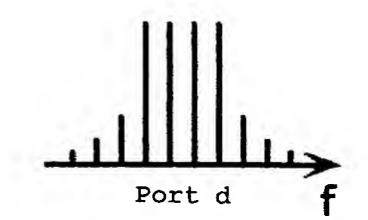


Fig. 13 (d)

